

# **User's Guide For SBC-9307-II**

**Rev 4.0**

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## Table of Contents

<b>1. Overview</b> .....	3
1.1. Product Views .....	3
1.2. Board Measurements .....	4
1.3. Introduction .....	5
1.4. Board Block Diagram .....	6
1.5. Features and Benefits Summary .....	7
<b>2. Board Details</b> .....	8
2.1. Parts Placement Diagram .....	8
2.2. CPU .....	9
2.3. SDRAM .....	9
2.4. FLASH .....	9
2.5. Power Supply (CN5) .....	10
2.6. Boot (JP1) .....	10
2.7. Serial Ports (COM1~COM7) .....	10
2.8. JTAG .....	12
2.9. KEYPAD (CN12) .....	12
2.10. USB (CN7、CN8) .....	13
2.11. LCD and TOUCH (CN4、CN9、JP3、JP4、JP5) .....	14
2.12. CAN-BUS (CAN1) .....	17
2.13. LED (D1、D2、D6、D7) .....	18
2.14. AUDIO (CN1) .....	18
2.15. Ethernet Port (RJ45) .....	18
2.16. GPIO (CN2) .....	19
2.17. CRT (VGA) .....	19
2.18. RESET (JP6) .....	19
2.19. Real-Time Clock .....	20
2.20. Watchdog Timer .....	20
2.21. CPLD (CPLD_J1) .....	20
<b>Revision History</b> .....	21

## **1. Overview**

### **1.1. Product Views**

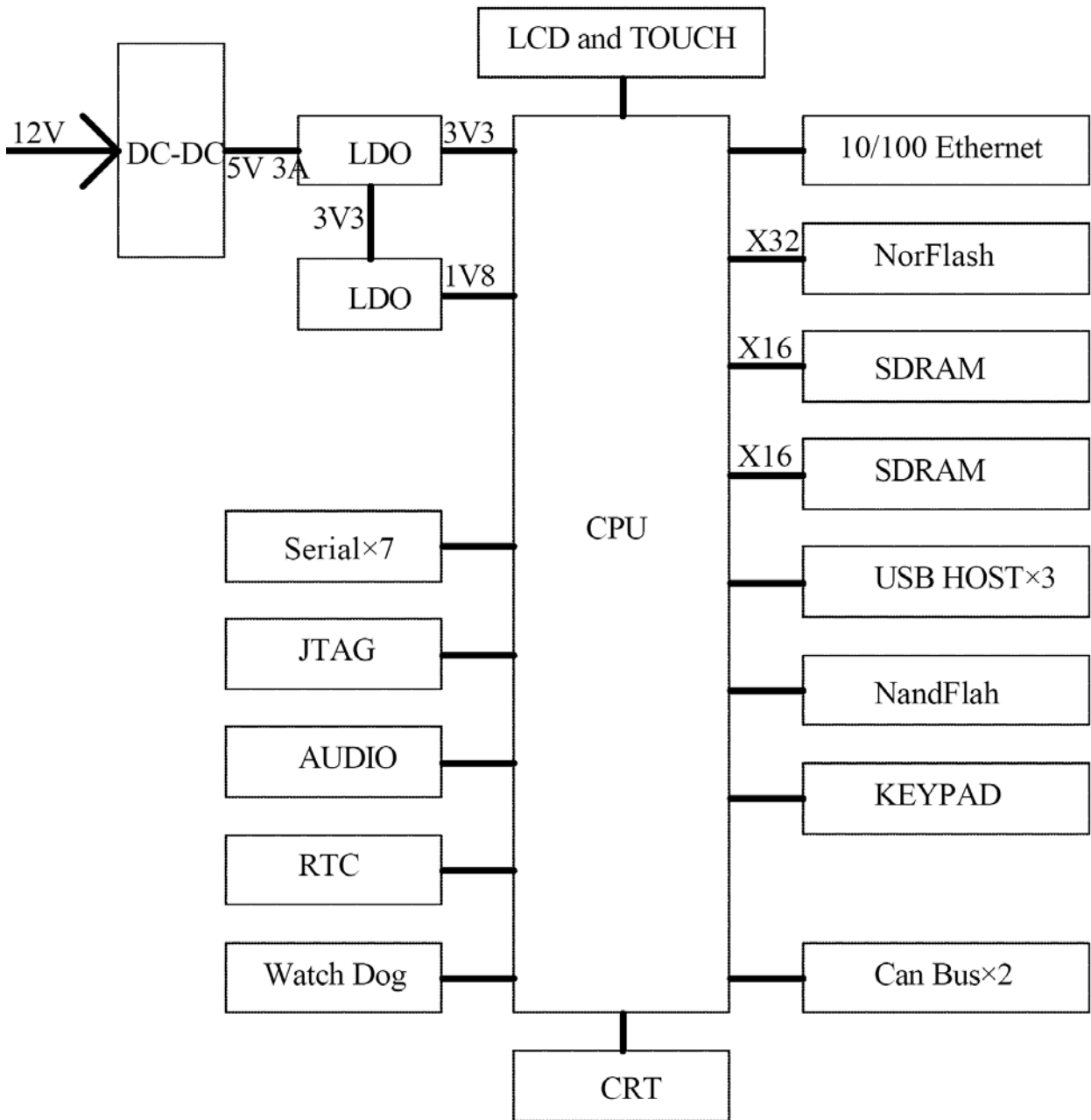


## 1.3. Introduction

The model SBC-9307-II is a compact, full-featured Single Board Computer (SBC) based on the Cirrus EP9307 ARM9 CPU. The EP9307 features an advanced 200 MHz ARM920T processor design with a memory management unit (MMU) that allows support for highlevel operating systems such as Linux, Windows CE, and other embedded operating systems. The ARM920T's 32-bit architecture, with a five-stage pipeline, delivers very impressive performance at very low power.

The EP9307 CPU has a 16 KB instruction cache and a 16 KB data cache to provide zero-cycle latency to the current program and data, or they can be locked to guarantee no-latency access to critical sections of instructions and data. For applications with instruction-memory size restrictions, the ARM920T's compressed Thumb instruction set can be used to provide higher code density and lower Flash storage requirements. The EP9307 CPU integer performance at 200 MHz is about twice as fast as the Technologic Systems 133MHz 586-based products, but costs half as much!

### 1.4. Board Block Diagram

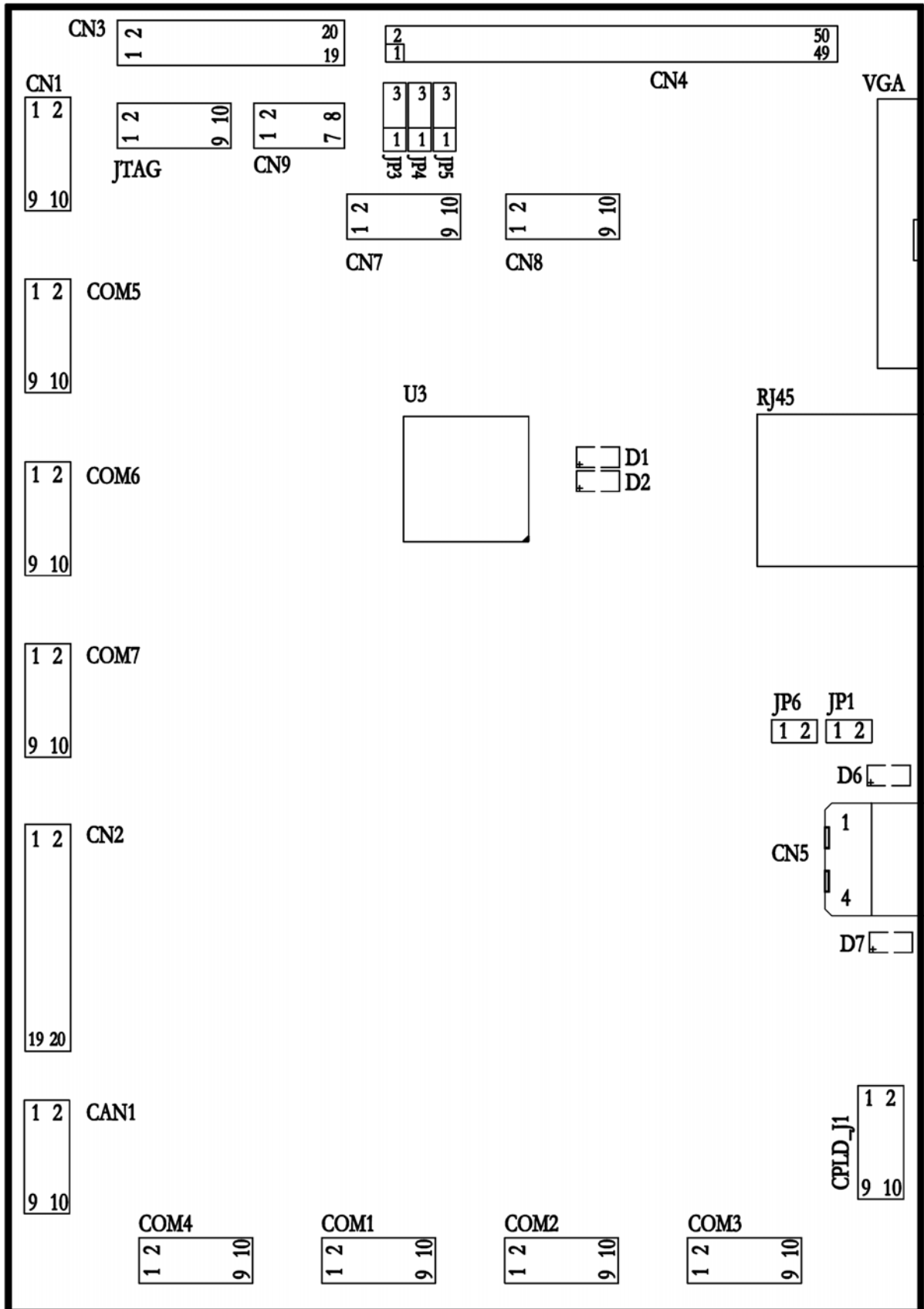


## 1.5. Features and Benefits Summary

- 200 MHz ARM9 CPU (EP9307) with MMU
- 64MB SDRAM at 100MHz
- 32MB NorFlash
- 32MB or 64MB NandFlash
- 10/100 Megabit Ethernet port
- 3 USB 2.0 compliant Full Speed host (OHCI) ports -- (12 Mb/s max)
- 7 COM ports (up to 115.2 Kbaud)
- Real-time clock (RTC)
- External watchdog (1.6s)
- 8x8 matrix keypad Interface
- Touch Screen Interface
- Alphanumeric LCD Interface and CRT Interface
- AC' 97 Interface
- 2 Can-Bus Interface
- Single +12VDC supply
- Small size -- (102x 146mm)

## 2. Board Details

### 2.1. Parts Placement Diagram



## 2.2. CPU

The EP9307 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Thin Client Computers for Business and Home
- Internet Radio
- Internet Access Devices
- Industrial Computers
- Specialized Terminals
- Point-of-sale Terminals
- Test and Measurement Equipment

The ARM920T microprocessor core with separate 16-kbyte, 64-way set-associative instruction and data caches is augmented by the MaverickCrunch™ coprocessor, enabling high-speed floating point calculations. MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100-Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, I2S audio, Raster/LCD, keypad, and touchscreen. A three-port USB 2.0 Full Speed Host (OHCI) (12 Mbits per second) and three UARTs are included as well. The EP9307 is a high-performance, low-power, RISCbased, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 200 MHz. The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 Mw and 750 mW (dependent on speed).

## 2.3. SDRAM

The SBC-9307-II uses a 256 Megabit SDRAM chip to provide 64 Megabytes (MB) of high-speed RAM. The SBC-9307-II SDRAM chip is soldered directly to the board. By not using socketed memory, the SBC-9307-II is much more reliable in high-vibration environments.

The SBC-9307-II RAM is not contiguous in the physical memory map of the EP9307. But the MMU is programmed to remap the blocks of RAM to appear as a contiguous block of memory at the very beginning of the virtual memory map. In the case of a 256 Megabit SDRAM chip (64 MB), it is located at 0 through 64 MB in the virtual memory map.

## 2.4. FLASH

The SBC-9307-II uses two Intel 3.3V StrataFlash chips for its on-board Flash resource. For the standard 16 Megabyte chip. The designer should be aware that Flash technology does have a wear-out mechanism that should be considered in all designs. The Intel Strata Flash memory is guaranteed capable of a minimum of 100,000 write/erase cycles. This

means that if you completely erase and rewrite the entire Flash drive 10 times a day, it would take over 27 years before any problems would occur. Reading the Flash produces no wear at all.

The SBC-9307-II use an another flash-NandFlash.the EP9307 CPU controls the NandFlash with GPIO and data bus.

## 2.5. Power Supply (CN5)


The SBC-9307-II requires regulated 12VDC at 800 mA (typical maximum),and the power is proteced by TVS .if use other external devices,such as :

- LCD
- USB

SBC-9307-II must requires a power over 800mA.

1	NC
2	GND
3	GND
4	+12V

+12V :Power input (Can use 6VDC~12VDC)

	<p><b>Warning</b> Supply voltagues over 13.5 VDC may damage the SBC-9307-II.</p>
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## 2.6. Boot (JP1)

JP1 for boot mode select.

Boot from UART :Cosed JP1

Boot from FLASH : Opend JP1

## 2.7. Serial Ports (COM1~COM7)

The EP9307 has three Three 16550-compatible UARTS ports :

- UART1 supports modem bit rates up to 115.2 Kbps,supports HDLC and includes a 16-byte FIFO for receive and a 16-byte FIFO for transmit. Interrupts are generated on Rx, Tx, and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 Kbps), medium (0.576 or 1.152Mbps), or fast (4 Mbps) IR data rates. It also has a 16-byte FIFO for receive and a 16-byte FIFO for transmit.
- UART3 supports HDLC and includes a 16-byte FIFO for receive and a 16-byte FIFO for transmit.

Interrupts are generated on Rx and Tx.

The SBC-9307-II has seven serial ports provide a means to communicate with external serial devices. All COM ports can support all standard baud rates up through 115.2K baud.

There are two 3-wire Communication Connectors(COM6~COM7) and five 9-wire Communication Connectors(COM1~COM5) in the SBC-9307-II

#### Pin-Outs Table:

##### COM1~COM4

DCD	1	2	RXD
TXD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

##### COM5

DCD0	1	2	RXD0
TXD0	3	4	DTR0
GND	5	6	DSR0
RTS0	7	8	CTS0
RI0	9	10	NC

##### COM6

NC	1	2	RXD1
TXD1	3	4	NC
GND	5	6	NC
NC	7	8	NC
NC	9	10	NC

##### COM7

NC	1	2	RXD2
TXD2	3	4	NC
GND	5	6	NC
NC	7	8	NC
NC	9	10	NC

## 2.8. JTAG

The JTAG interface is the standard 10-Pin debugging emulator interface, and it allows use of ARM's Multi-ICE or other in-circuit emulators.

### Pin-Outs Table:

VDD33	1	2	VDD33
TRST	3	4	nRESET
TDI	5	6	GND
TMS	7	8	TDO
TCK	9	10	TCK

## 2.9. KEYPAD (CN12)

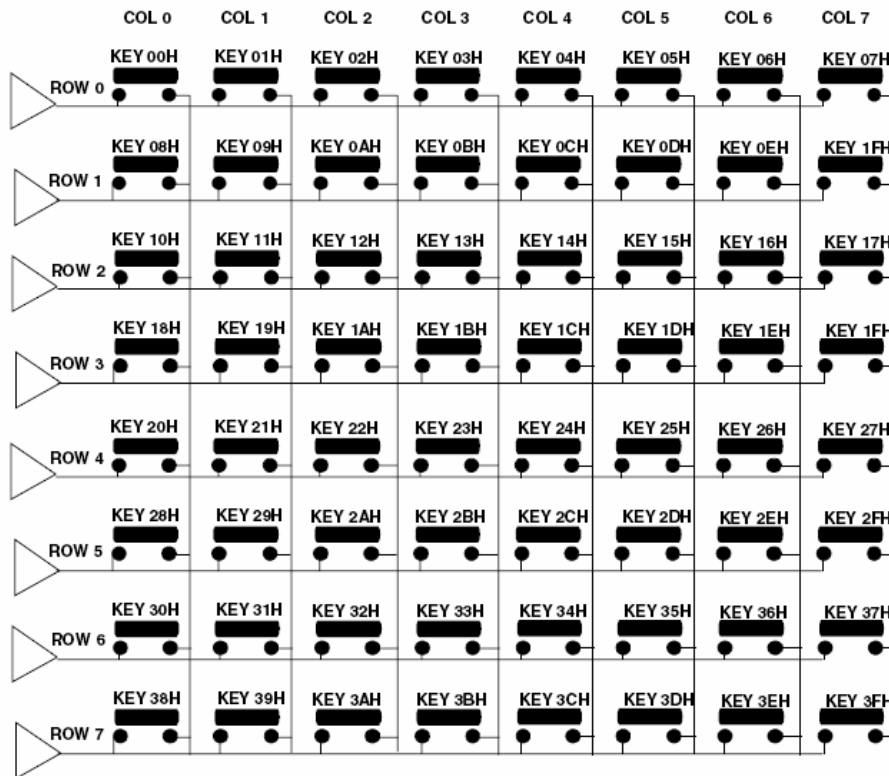
The keypad circuitry scans an 8 x 8 array of 64 normally open, single pole switches. Any one or two keys depressed will be de-bounced and decoded. An interrupt is generated whenever a stable set of depressed keys is detected. If the keypad is not utilized, the 16 column/row pins may be used as general purpose I/O. The Keypad interface:

- Provides scanning, debounce and decoding for a 64-key array.
- Scans an 8-row by 8-column matrix.
- May decode 2 keys at once.
- Generates an interrupt when a new stable key is determined.
- Also generates a 3-key reset interrupt.

### Pin-Outs Table:

VDD33	1	2	VDD33
COL0	3	4	COL1
COL2	5	6	COL3
COL4	7	8	COL5
COL6	9	10	COL7
ROW0	11	12	ROW1
ROW2	13	14	ROW3
ROW4	15	16	ROW5
ROW6	17	18	ROW7
GND	19	20	GND

VDD33 : Power output



## 2.10. USB (CN7、CN8)

The USB Open Host Controller Interface (Open HCI) provides full speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tieredstar” topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus The Open HCI host controller initializes the

### Pin-Outs Table:

CN7

VDD50	1	2	VDD50
USBM0-	3	4	USBM1-
USBP0+	5	6	USBP1+
GND	7	8	GND
NC	9	10	NC

CN8

VDD50	1	2	NC
USBM2-	3	4	NC
USBP2+	5	6	NC
GND	7	8	NC
NC	9	10	NC

## 2.11. LCD and TOUCH (CN4、CN9、JP3、JP4、JP5)

The EP9307 Raster/LCD interface provides data and interface signals for a variety of display types. It features fully programmable video interface timing for non-interlaced flat panel or dual scan displays. Resolutions up to 1280 x 1024 are supported from a unified SDRAM based frame buffer. A 16-bit PWM provides control for LCD panel contrast. LCD specific features include:

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dualscan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 18-bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low end panel.

THE EP9307 Touch Screen Interface has 12-bit Analogto-Digital Converter (ADC) The touch screen interface performs all sampling, averaging, ADC range checking, and control for a wide variety of analog resistive touch screens. This controller only interrupts the processor when a meaningful change occurs. The touch screen hardware may be disabled and the switch matrix and ADC controlled directly if desired. Features include:

- Support for 4, 5, 7, or 8-wire analog resistive touch screens.
- Flexibility - unused lines may be used for temperature sensing or other functions.
- Touch screen interrupt function.

**Pin-Outs Table:**

## LCD

+12V	1	2	+12V
GND	3	4	GND
VDD_LCD	5	6	VDD_LCD
GND	7	8	GND
NC	9	10	NC
B0(P0)	11	12	B1(P1)
B2(P2)	13	14	B3(P3)
B4(P4)	15	16	B5(P5)
NC	17	18	NC
G0(P6)	19	20	G1(P7)
G2(P8)	21	22	G3(P9)
G4(P10)	23	24	G5(P11)
NC	25	26	NC
R0(P12)	27	28	R1(P13)
R2(P14)	29	30	R3(P15)
R4(P16)	31	32	R5(P17)
U/L	33	34	R/L
DCLK	35	36	VSYNC
DENB	37	38	HSYNC
BRIGHT	39	40	EGPIO1
GND	41	42	GND
XM	43	44	XP
SXM	45	46	SXP
YM	47	48	YP
SYM	49	50	SYP

+12V :Output +12V from power input

R :RED

G :GREEN

B :BLUE

EGPIO1 :Output,active high

BRIGHT :PWM

DENB : Enable

VSYNC : Vertical Synchronous Signal

HSYNC : Horizontal Synchronous Signal

DCLK : Clock Signal for Sampling Image Digital Data



### Warning

Using an incorrect cable or mounting the LCD connector on the front-side can result in a reverse power polarity and can damage the LCD display. Please refer to your LCD data sheets for in-depth information.

JP3 (Power for LCD)

1	VDD50
2	VDD_LCD
3	VDD33

JP4 (select for R/L)

1	Pull-Up
2	R/L
3	Pull-Down

JP5 (select for U/L)

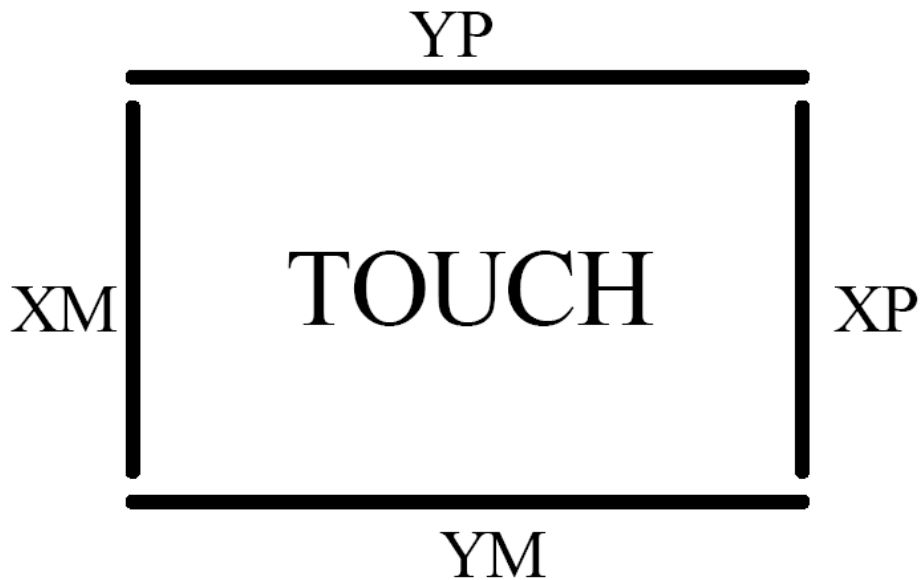
1	Pull-Up
2	U/L
3	Pull-Down

Pull-Up :Pull-up 10K resistor at VDD\_LCD

Pull-Down :Pull-down 10K resistor at GND

TOUCH (CN9)

YP	1	2	SYP
YM	3	4	SYM
XP	5	6	SXP
XM	7	8	SXM

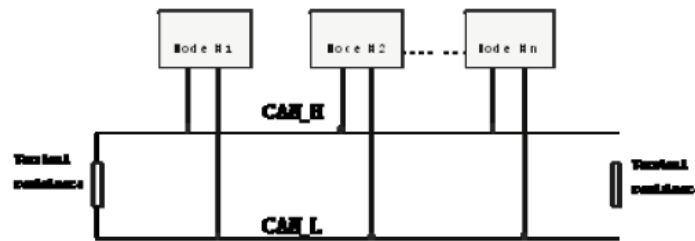


## 2.12.CAN-BUS (CAN1)

The SBC-9307-II has two CAN-bus used SJA1000 and a module , Features include:

- CAN 2.0B
- Can-bus power supply with DC/DC converter
- ESD protection
- Photocoupler protection

To connect SBC-9307-II CAN-bus module to the CAN-bus, user only need to connect CAN\_L and CAN\_L, CAN\_H and CAN\_H.CAN-bus network adopts straight-line topology, and two terminal 120Ω resistances need to be installed on the two bus terminals. If the number of nodes larger than 2, the 120Ω resistance is not necessary to be installed on the middle node. The length of branch connection should not be longer than 3 meters. The connections for the CAN-bus are shown:

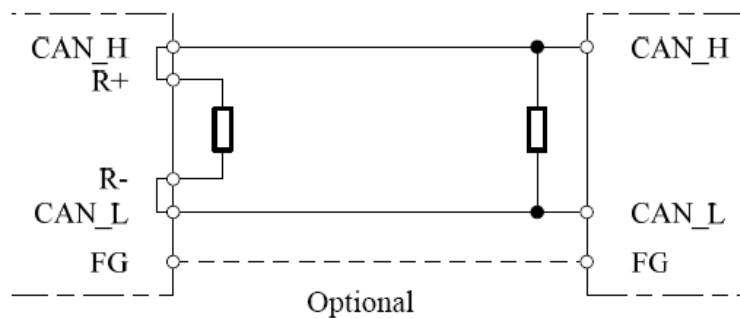


Note: CAN-bus cable can be either ordinary twisted-pair or shield twisted-pair. If the communication distance is longer than 1Km, then the area of section for the twisted-pair should be larger than  $\Phi 1.0\text{mm}^2$  . The particular specification depends upon the communication distance, and a longer distance usually requires a larger area.

To enhance the reliability for the CAN communication, two terminal resistances need to be respectively installed on to the two terminals on the CAN bus network, see above. The value for the terminal match resistance depends on the characteristic resistance of the transfer cable. For example, the characteristic resistance of the twisted-pair is 120Ω, so the terminal resistance on the bus terminal should be also 120Ω.

For SBC-9307-II CAN-bus intelligent interface, it is necessary to add external terminal resistance, because each CAN channel has not internally integrated a 120Ω terminal resistance. When SBC-9307-II CAN-bus interface locates on one of the nodes on the network, a 120Ω terminal resistance needs to be respectively connected to “R\_H” and “R\_L” pins.

See that:



**R+ = R\_H**

**R- = R\_L**

**FG = GND(shield)**

**Pin-Outs Table:**

SHIELD	1	2	SHIELD
R_0_L	3	4	R_1_L
R_0_H	5	6	R_1_H
CAN_0_L	7	8	CAN_1_L
CAN_0_H	9	10	CAN_1_H

**2.13.LED (D1、 D2、 D6、 D7)**

The led designed to show the CPU status and power status.

D1 : CPU LED

D2 : CPU LED

D6 : VDD50 LED

D7 : VDD33 LED

**2.14.AUDIO (CN1)**

A AC' 97 audio CODEC is used to support the audio features of the SBC-9307-II.Audio inputs and output supported by the CS4202 are stereo line out and line in ,and it supported a mono microphone input.

**Pin-Outs Table:**

OUT_R	1	2	OUT_L
AGND	3	4	AGND
IN_R	5	6	IN_L
AGND	7	8	AGND
MIC_IN_R	9	10	MIC_IN_L

**2.15.Ethernet Port (RJ45)**

The EP9307 has a Ethernet MAC,the MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported.Features include:

- Supports 1/10/100 Mbps transfer rates for home /small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

The EP9307 Ethernet LAN controller incorporates all the logic needed to interface directly to any MII compatible Ethernet PHY chip. A low-power Micrel KS8721 chip is used to implement the Ethernet PHY function and an

integrated RJ-45 connector with built-in 10/100 transformer and LED indicators completes the Ethernet sub-system.

## 2.16.GPIO (CN2)

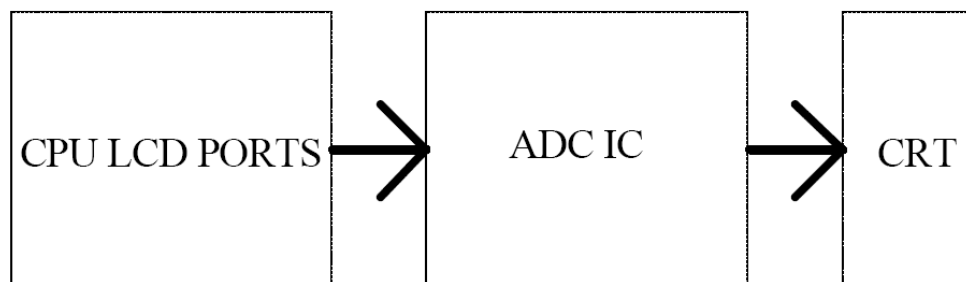
GPIO expansion interface, used to external function expansion.

### Pin-Outs Table:

VDD33	1	2	VDD33
HGPIO7	3	4	EGPIO9
HGPIO6	5	6	NC
HGPIO5	7	8	NC
HGPIO4	9	10	GND
HGPIO3	11	12	GND
HGPIO2	13	14	GND
SLA0	15	16	GND
PWM0	17	18	GND
VDD33	19	20	VDD33

## 2.17. CRT (VGA)

The SBC-9307-II supports a CRT interface ,this will allow to connect it to the CRT displays.The designer is that:



The ADC IC (adv7123) is a triple high speed, digital-to-analog converter on a single monolithic chip. It consists of three high speed, 10-bit, video D/A converters with complementary outputs, a standard TTL input interface and a high impedance, analog output current source.The SBC-9307-II CRT supports up to 1024x768 at 85MHz.

## 2.18. RESET (JP6)

### Pin-Outs Table:

1	nMR
2	GND

JP6 :Cosed JP6 reset the system

## 2.19. Real-Time Clock

The SBC-9307-II has an option for a real-time clock (RTC). This option (PCF8563) is a CMOS real-time clock/calendar optimized for low power consumption. This module contains the 3.0 V lithium battery, 32.768 kHz crystal, and a RTC chip. It is low back-up current; typical 0.25 mA at VDD = 3.0 V and Tamb = 25 °C.

## 2.20. Watchdog Timer

The SBC-9307-II implements a watchdog timer (WDT) unit. The WDT can be used to prevent a system “hanging” due to a software failure. The WDT causes a full system reset when the WDT times out, allowing a guaranteed recovery time from a software error. To prevent a WDT timeout, the application must periodically “feed” the WDT by writing a specific value to a specific memory location.

The WDT Control register must be initialized with the timeout period desired. This may be as short as 1.6 seconds. After the WDT has been enabled, the WDT counter starts counting. The application software can reset this counter at any time by “Feeding the WDT”.If the WDT counter reaches the timeout period, then a full system reset occurs.

## 2.21.CPLD (CPLD\_J1)

Use it to program CPLD IC.

### Pin-Outs Table:

TCK	1	2	GND
TDO	3	4	VDD33
TMS	5	6	NC
NC	7	8	NC
TDI	9	10	GND

## Revision History

<b>Version</b>	<b>Modifications</b>
Rev 1.0	Initial version
Rev 2.0	
Rev 3.0	
Rev 4.0	Update all