

User's Guide For SBC-9315

Rev 3.0

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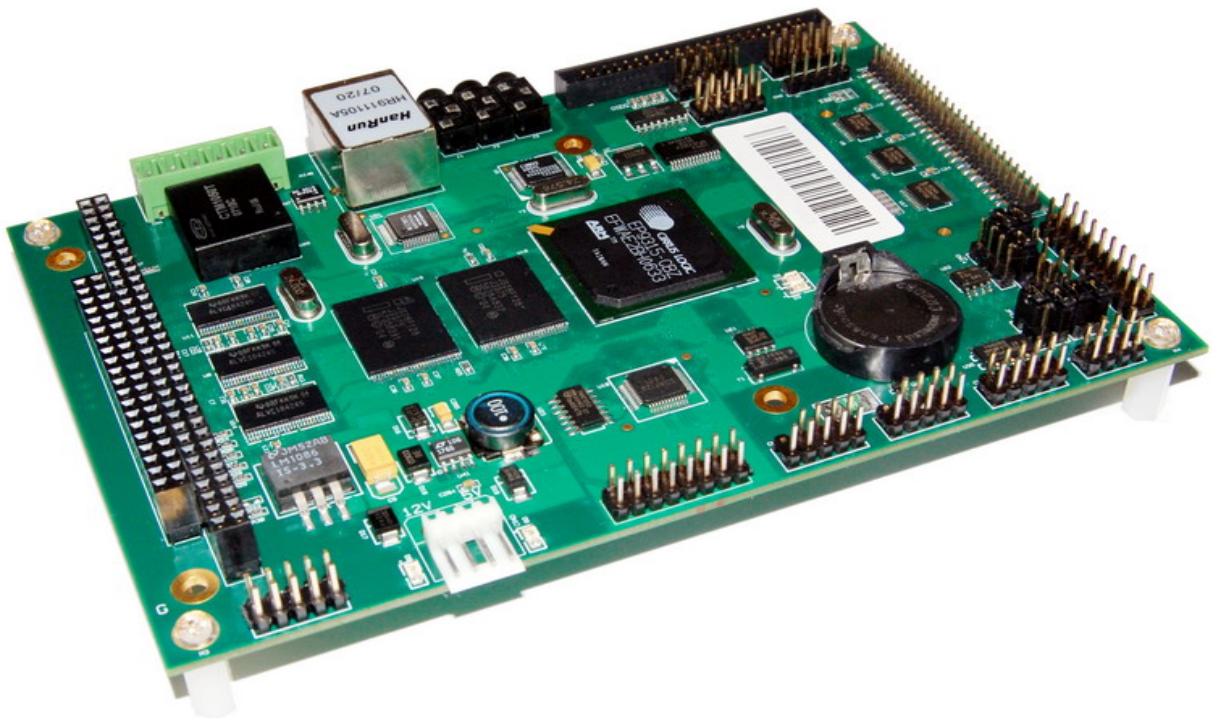
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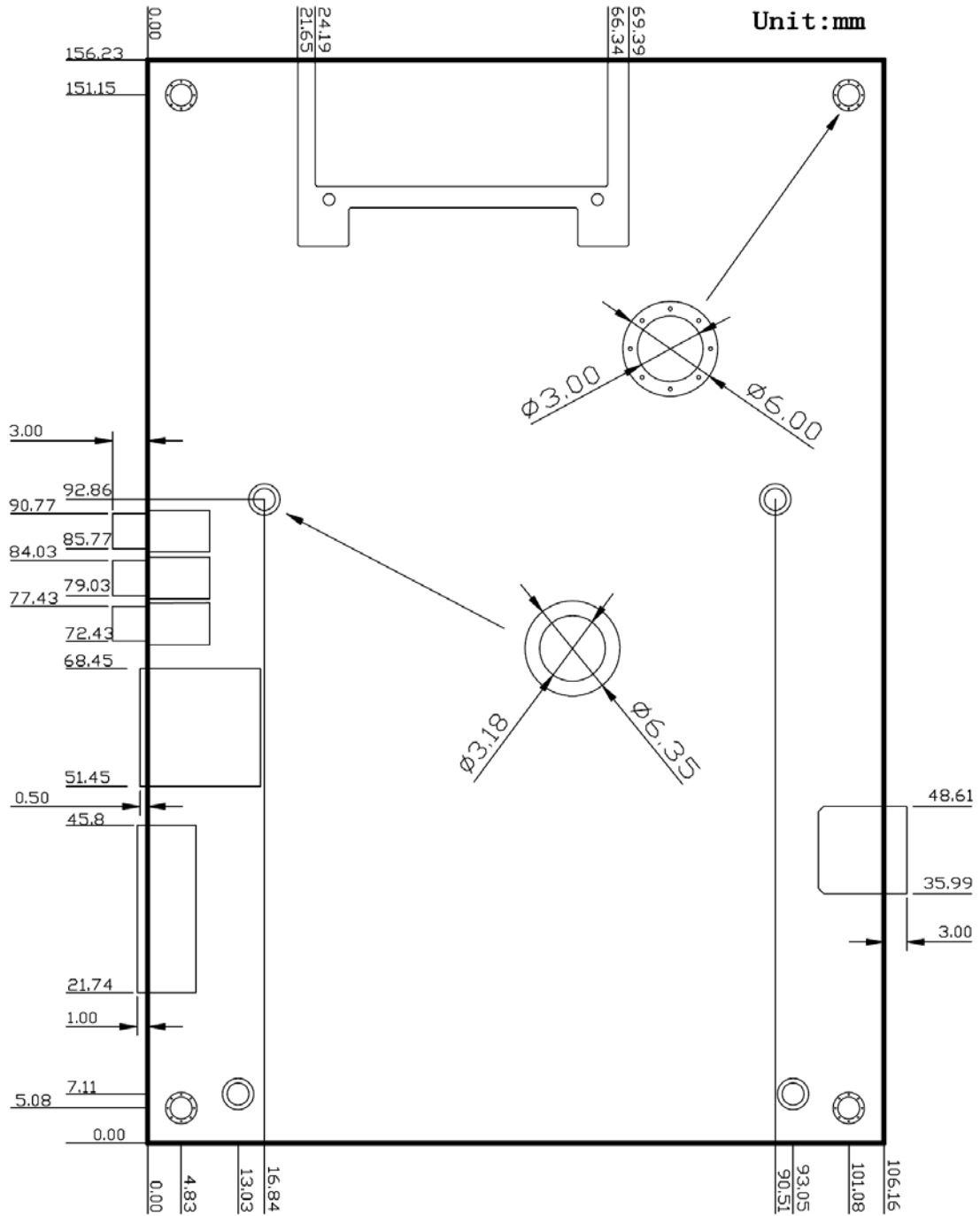
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1. Overview

1.1. Product Views



1.2. Board Measurements

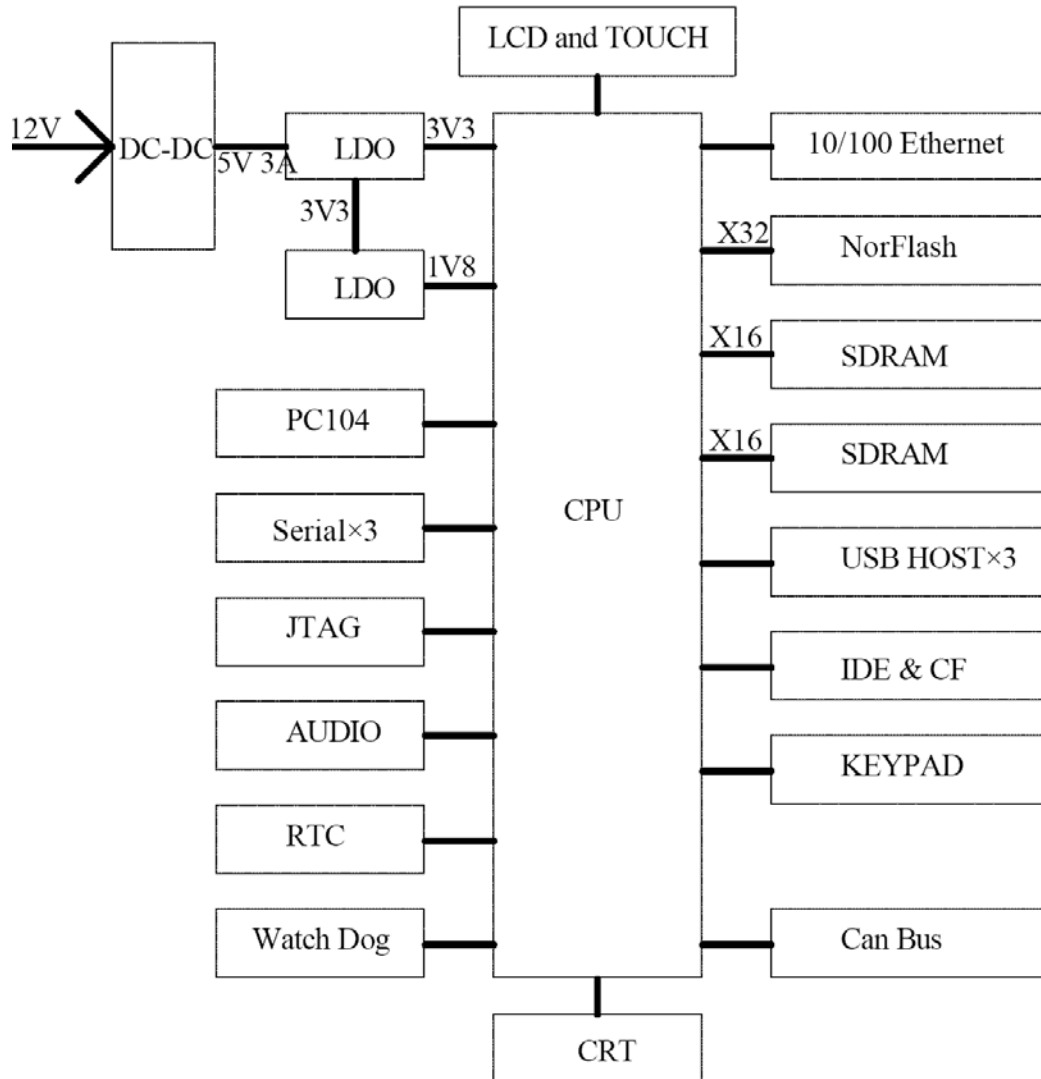


1.3. Introduction

The model SBC-9315 is a compact, full-featured Single Board Computer (SBC) based on the Cirrus EP9315 ARM9 CPU. The EP9315 features an advanced 200 MHz ARM920T processor design with a memory management unit (MMU) that allows support for highlevel operating systems such as Linux, Windows CE, and other embedded operating systems. The ARM920T's 32-bit architecture, with a five-stage pipeline, delivers very impressive performance at very low power.

The EP9315 CPU has a 16 KB instruction cache and a 16 KB data cache to provide zero-cycle latency to the current program and data, or they can be locked to guarantee no-latency access to critical sections of instructions and data. For applications with instruction-memory size restrictions, the ARM920T's compressed Thumb instruction set can be used to provide higher code density and lower Flash storage requirements. The SBC-9315 CPU integer performance at 200 MHz is about twice as fast as the Technologic Systems 133MHz 586-based products, but costs half as much!

1.4. Board Block Diagram

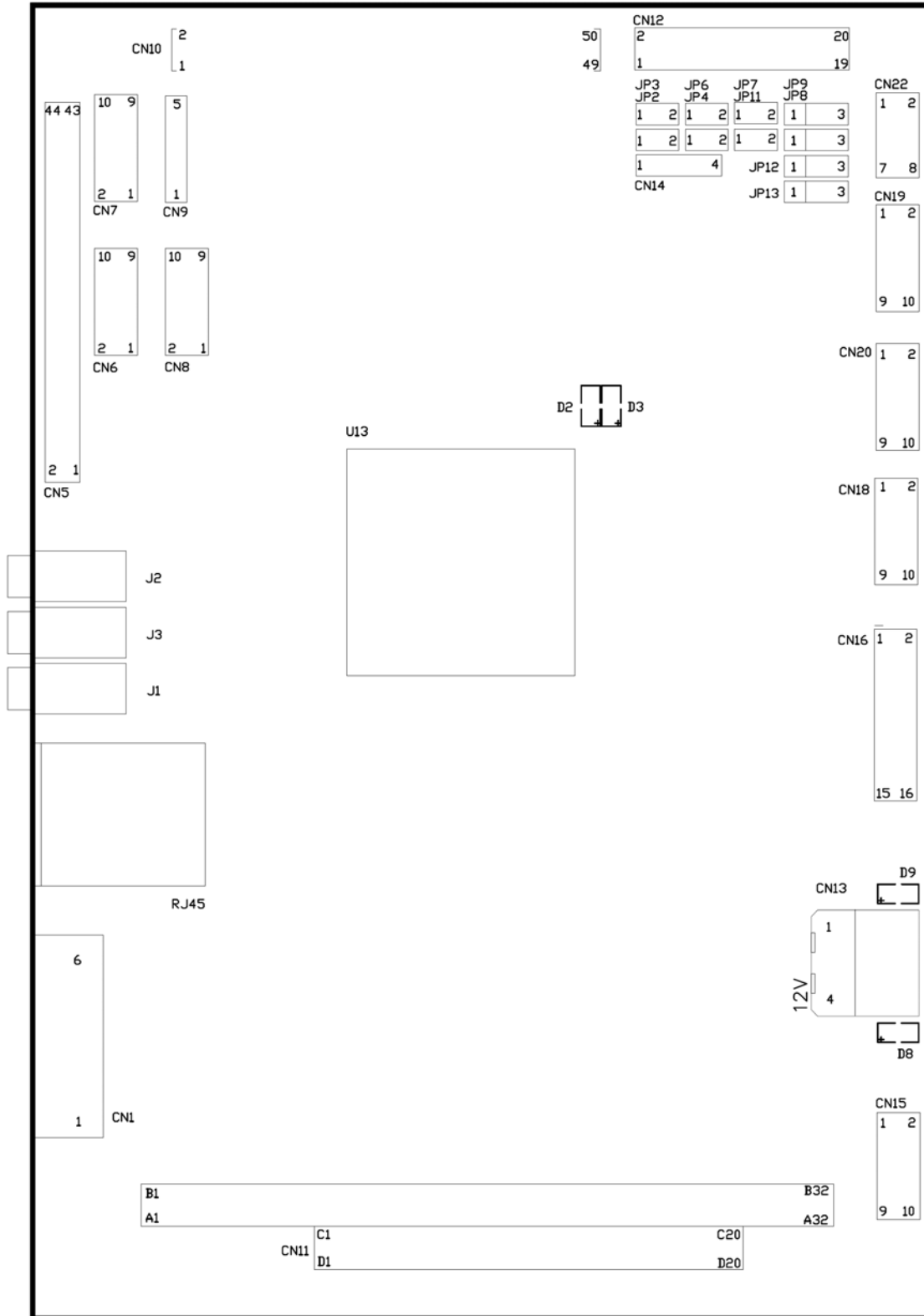


1.5. Features and Benefits Summary

- 200 MHz (184 MHz for industrial) ARM9 CPU (EP9315) with MMU
- 64MB SDRAM at 100MHz
- 32MB NorFlash
- True IDE Compact Flash socket and IDE socket
- 10/100 Megabit Ethernet port
- 3 USB 2.0 compliant Full Speed host (OHCI) ports -- (12 Mb/s max)
- 3 COM ports (up to 115.2 Kbaud)
- PC/104 expansion bus
- Real-time clock (RTC)
- External watchdog (1.6s)
- 8x8 matrix keypad Interface
- Touch Screen Interface
- Alphanumeric LCD Interface and CRT Interface
- AC' 97 Interface
- 1 Can-Bus Interface
- Single +12VDC supply
- Small size -- (106.1x 156.2 mm)

2. Board Details

2.1. Parts Placement Diagram



2.2. CPU

The EP9315 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Thin Client Computers for Business and Home
- Internet Radio
- Internet Access Devices
- Industrial Computers
- Specialized Terminals
- Point-of-sale Terminals
- Test and Measurement Equipment

The ARM920T microprocessor core with separate 16-kbyte, 64-way set-associative instruction and data caches is augmented by the MaverickCrunch™ coprocessor, enabling high-speed floating point calculations. MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100-Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, I2S audio, Raster/LCD, IDE storage peripherals, keypad, and touchscreen. A three-port USB 2.0 Full Speed Host (OHCI) (12 Mbits per second) and three UARTs are included as well. The EP9315 is a high-performance, low-power, RISCbased, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 200 MHz (184 MHz for industrial conditions). The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 Mw and 750 mW (dependent on speed).

2.3. SDRAM

The SBC-9315 uses a 512 Megabit SDRAM chip to provide 64 Megabytes (MB) of high-speed RAM. The SBC-9315 SDRAM chip is soldered directly to the board. By not using socketed memory, the SBC-9315 is much more reliable in high-vibration environments.

The SBC-9315 RAM is not contiguous in the physical memory map of the EP9315. But the MMU is programmed to remap the blocks of RAM to appear as a contiguous block of memory at the very beginning of the virtual memory map. In the case of a 512 Megabit SDRAM chip (64 MB), it is located at 0 through 64 MB in the virtual memory map.

2.4. FLASH

The SBC-9315 uses two Intel 3.3V StrataFlash chips for its on-board Flash resource. For the standard 16 Megabyte chip. The designer should be aware that Flash technology does have a wear-out mechanism that should

be considered in all designs. The Intel Strata Flash memory is guaranteed capable of a minimum of 100,000 write/erase cycles. This means that if you completely erase and rewrite the entire Flash drive 10 times a day, it would take over 27 years before any problems would occur. Reading the Flash produces no wear at all.

2.5. Power Supply (CN13)

The SBC-9315 requires regulated 12VDC at 600 mA (typical maximum),and the power is proteced by TVS .if use other external devices,such as :

- LCD
- IDE
- CF CARD
- PC104

SBC-9315 must requires a power over 600mA.

1	NC
2	GND
3	GND
4	+12V

+12V :Power input (Can use 6VDC~12VDC)

Warning



Supply voltages over 12 VDC may damage the SBC-9315.

2.6. Boot (JP2、JP3)

JP2 and JP3 for boot mode select.

Boot from UART :Cosed JP3 and Opened JP2

Boot from FLASH : Cosed JP2 and JP3

2.7. Serial Port (CN6、CN7、CN8、CN9、CN14)

The EP9315 has three Three 16550-compatible UARTS ports :

- UART1 supports modem bit rates up to 115.2 Kbps,supports HDLC and includes a 16-byte FIFO for receive and a 16-byte FIFO for transmit. Interrupts are generated on Rx, Tx, and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 Kbps), medium (0.576 or 1.152Mbps), or fast (4 Mbps) IR data rates. It also has a 16-byte FIFO for receive and a 16-byte FIFO for transmit.
- UART3 supports HDLC and includes a 16-byte FIFO for receive and a 16-byte FIFO for

transmit. Interrupts are generated on Rx and Tx.

The SBC-9315 has three serial ports provide a means to communicate with external serial devices. All COM ports can support all standard baud rates up through 115.2K baud.

Pin-Outs Table:

CN6 (COM2)

NC	1	2	RXD2
TXD2	3	4	NC
GND	5	6	NC
NC	7	8	NC
NC	9	10	NC

CN7 (COM0)

DCD0	1	2	RXD0
TXD0	3	4	DTR0
GND	5	6	DSR0
RTS0	7	8	CTS0
RI0	9	10	NC

CN8 (COM1)

NC	1	2	RXD1
TXD1	3	4	NC
GND	5	6	NC
NC	7	8	NC
NC	9	10	NC

CN9 (IrDA) (NOT USE)

1	VDD33
2	RXD1
3	TXD1
4	EGPIO9
5	GND

CN14 (RS485) (NOT USE)

1	B
2	A
3	NC
4	GND

2.8. CF and IDE (CN21、CN5、JP4、JP6、JP8)

The IDE Interface and CF card Interface provide an industry-standard connection to two AT Advanced Packet Interface (ATAPI) compliant devices. The IDE port will attach to a master and a slave device. The internal DMA controller performs all data transfers using the Ultra DMA modes. The interface supports the following operating modes:

- ▣ PIO Mode 0 thru 4
- ▣ Ultra DMA Modes 0 thru 3

Pin-Outs Table:

CN5 :IDE interface

JP6 :Cosed JP6 make IDE work in the primary mode,
Opened JP6 make IDE work in the salve mode,

JP8 (Power for CF card)

1	VDD50
2	VDD_CF
3	VDD33

JP4 : Cosed JP4 make CF card works in the primary mode,
Opened JP4 make CF card works in the salve mode,

2.9. JTAG (CN19)

VDD33	1	2	VDD33
TRST	3	4	nRESET
TDI	5	6	GND
TMS	7	8	TDO
TCK	9	10	TCK

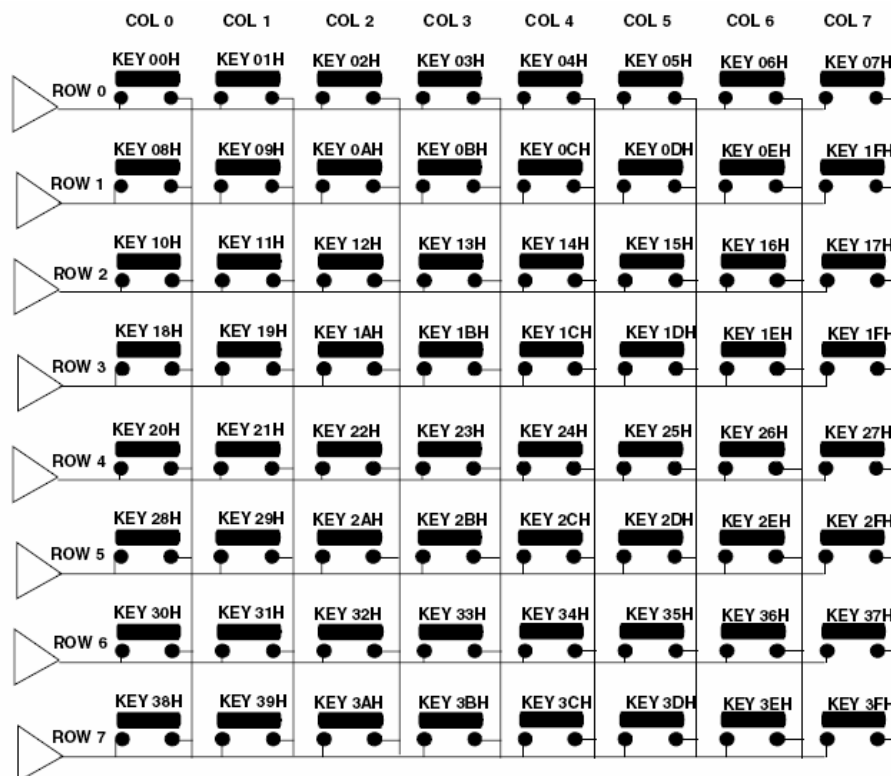
2.10. KEYPAD (CN12)

EP9315 Port C and port D signals COL0 thru COL7 and ROW0 thru ROW7 are physically arranged to allow a 20-pin (2x10) ribbon cable to directly connect a 8x8 matrix keypad.

Pin-Outs Table:

VDD33	1	2	VDD33
COL0	3	4	COL1
COL2	5	6	COL3
COL4	7	8	COL5
COL6	9	10	COL7
ROW0	11	12	ROW1
ROW2	13	14	ROW3
ROW4	15	16	ROW5
ROW6	17	18	ROW7
GND	19	20	GND

VDD33 : Power output



2.11. USB (CN18、CN20)

The USB Open Host Controller Interface (Open HCI) provides full speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tieredstart” topology.

This includes the following features:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections

- Root HUB integrated with 3 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus The Open HCI host controller initializes the

Pin-Outs Table:

CN18

VDD50	1	2	VDD50
USBM0-	3	4	USBM1-
USBP0+	5	6	USBP1+
GND	7	8	GND
NC	9	10	NC

CN20

VDD50	1	2	NC
USBM2-	3	4	NC
USBP2+	5	6	NC
GND	7	8	NC
NC	9	10	NC

2.12. LCD and TOUCH (CN10, CN22, JP9, JP12, JP13)

The EP9315 Raster / LCD interface provides data and interface signals for a variety of display types. It features fully programmable video interface timing for non-interlaced flat panel or dual scan displays. Resolutions up to 1024 x 768 are supported from a unified SDRAM based frame buffer. A 16-bit PWM provides control for LCD panel contrast. LCD specific features include:

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dualscan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 24 bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low end panel

THE EP9315 touch screen interface performs all sampling, averaging, ADC range checking, and control for a wide variety of analog resistive touch screens. This controller only interrupts the processor when a meaningful change occurs. The touch screen hardware may be disabled and the switch matrix and ADC controlled directly if desired.

Features include:

- Support for 4-, 5-, 7-, or 8-wire analog resistive touchscreens.
- Flexibility - unused lines may be used for temperature sensing or other functions.
- Touch screen interrupt function.

Pin-Outs Table:

LCD (CN10)

+12V	1	2	+12V
GND	3	4	GND
VDD_LCD	5	6	VDD_LCD
GND	7	8	GND
NC	9	10	NC
B0(P0)	11	12	B1(P1)
B2(P2)	13	14	B3(P3)
B4(P4)	15	16	B5(P5)
NC	17	18	NC
G0(P6)	19	20	G1(P7)
G2(P8)	21	22	G3(P9)
G4(P10)	23	24	G5(P11)
NC	25	26	NC
R0(P12)	27	28	R1(P13)
R2(P14)	29	30	R3(P15)
R4(P16)	31	32	R5(P17)
U/L	33	34	R/L
DCLK	35	36	VSYNC
DENB	37	38	HSYNC
BRIGHT	39	40	EGPIO1
GND	41	42	GND
XM	43	44	XP
SXM	45	46	SXP
YM	47	48	YP
SYM	49	50	SYP

+12V :Output +12V from power input

R :RED

G :GREEN

B :BLUE

EGPIO1 :Output, active high

BRIGHT :PWM
 DENB : Enable
 VSYNC : Vertical Synchronous Signal
 HSYNC : Horizontal Synchronous Signal
 DCLK : Clock Signal for Sampling Image Digital Data

Warning



Using an incorrect cable or mounting the LCD connector on the front-side can result in a reverse power polarity and can damage the LCD display. Please refer to your LCD data sheets for in-depth information.

JP9 (Power for LCD)

1	VDD50
2	VDD_LCD
3	VDD33

JP12 (select for R/L)

1	Pull-Up
2	R/L
3	Pull-Down

JP13 (select for U/L)

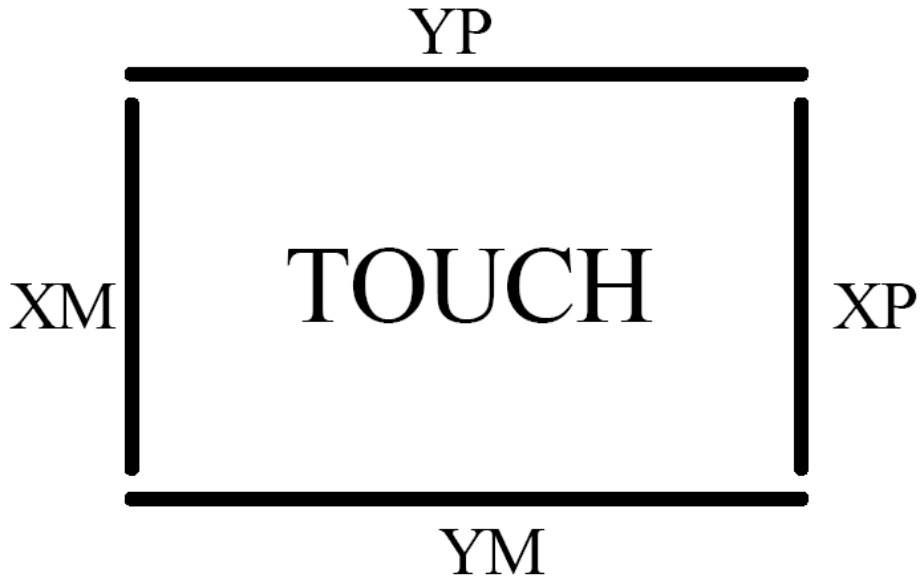
1	Pull-Up
2	U/L
3	Pull-Down

Pull-Up :Pull-up 10K resistor at VDD_LCD

Pull-Down :Pull-down 10K resistor at GND

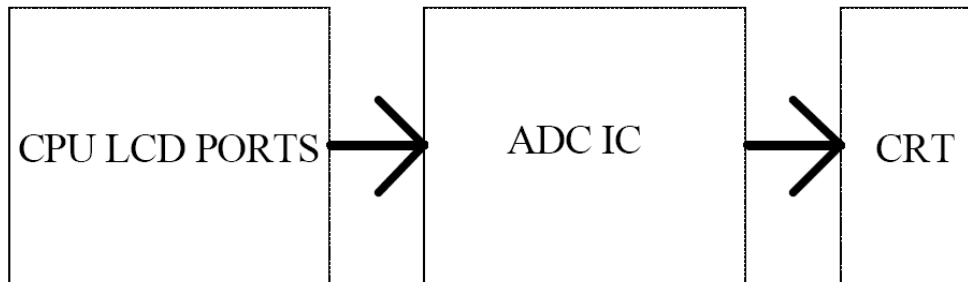
TOUCH (CN22)

YP	1	2	SYP
YM	3	4	SYM
XP	5	6	SXP
XM	7	8	SXM



2.13. CRT (CN16)

The SBC-9315 supports a CRT interface ,this will allow to connect it to the CRT displays.The designer is that:



Pin-Outs Table:

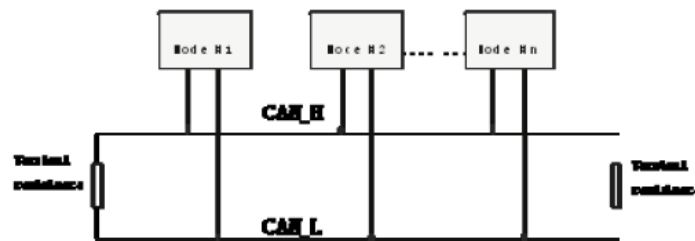
CRT_R	1	2	CRT_G
CRT_B	3	4	NC
GND	5	6	GND
GND	7	8	GND
NC	9	10	GND
NC	11	12	NC
CRT_HSYNC	13	14	CRT_VSYNC
NC	15	16	NC

2.14. CAN-BUS (CN1)

The SBC-9315 has one CAN-bus used SJA1000 and a module , Features include:

- CAN 2.0B
- Can-bus power supply with DC/DC converter
- ESD protection
- Photocoupler protection

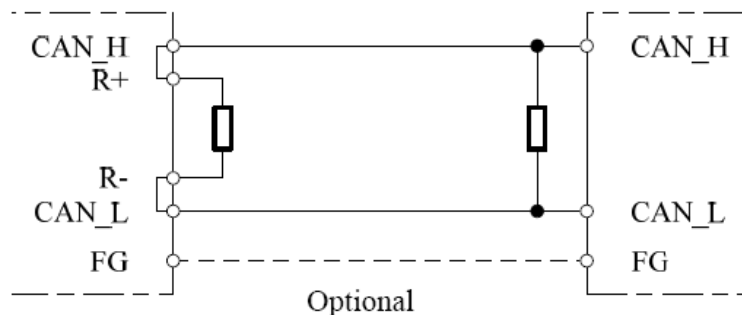
To connect SBC-9315 CAN-bus module to the CAN-bus, user only need to connect CAN_L and CAN_L, CAN_H and CAN_H.CAN-bus network adopts straight-line topology, and two terminal 120Ω resistances need to be installed on the two bus terminals. If the number of nodes larger than 2, the 120Ω resistance is not necessary to be installed on the middle node. The length of branch connection should not be longer than 3 meters. The connections for the CAN-bus are shown:



Note: CAN-bus cable can be either ordinary twisted-pair or shield twisted-pair. If the communication distance is longer than 1Km, then the area of section for the twisted-pair should be larger than $\Phi 1.0\text{mm}^2$. The particular specification depends upon the communication distance, and a longer distance usually requires a larger area.

To enhance the reliability for the CAN communication, two terminal resistances need to be respectively installed on to the two terminals on the CAN bus network, see above. The value for the terminal match resistance depends on the characteristic resistance of the transfer cable. For example, the characteristic resistance of the twisted-pair is 120Ω, so the terminal resistance on the bus terminal should be also 120Ω.

For SBC-9315 CAN-bus intelligent interface, it is necessary to add external terminal resistance, because each CAN channel has not internally integrated a 120Ω terminal resistance. When SBC-9315 CAN-bus interface locates on one of the nodes on the network, a 120Ω terminal resistance needs to be respectively connected to “R_H“ and “R_L” pins. See that:



- R+ = R_H**
- R- = R_L**
- FG = GND(Shield)**

Pin-Outs Table:

1	VDD50
2	CAN_H
3	CAN_L
4	R_H
5	R_L
6	GND

2.15. PC104 (CN11)

The PC/104 is a compact implementation of the PC/AT ISA bus ideal for embedded applications. Designers benefit from using an already-developed standard, rather than creating their own. Further, the presence of a compact form-factor PC compatible standard has encouraged the development of a broad array of off-the-shelf products, allowing a very quick time to market for new products.

The electrical specification for the PC/104 expansion bus is identical to the PC ISA bus. The mechanical specification allows for the very compact implementation of the ISA bus tailor made for embedded systems. The full PC/104 specification is available from the IEEE Standards Office under # IEEE P996.1 (see Appendix E for further information). Basically, this bus allows multiple daughter boards in a 3.6 inch by 3.8 inch form factor to be added in a self-stacking bus. Since the electrical specs are identical (except for drive levels) to a standard PC ISA bus, standard peripherals such as COM ports, Digital I/O, Ethernet ports, and LCD drivers may be easily added..

The SBC-9315 implements a sub-set of the full PC/104 bus. This allows the support of many common I/O daughter boards. Some of the PC/104 signals are not supported such as the DMA signals. And it supports 8-bit data bus or 16-bit data bus.

0x10000000 –	Read address, read the data to decide which IRQ
0x30000000 – 0x30FFFFFF	PC/104 memory space (16MB)
0x31000000 – 0x310003FF	PC/104 I/O space (1kB)

Pin-Outs Table:

NC	A1	B1	GND
D7	A2	B2	RESET
D6	A3	B3	VDD50
D5	A4	B4	IRQ9
D4	A5	B5	NC
D3	A6	B6	NC
D2	A7	B7	NC
D1	A8	B8	NC
D0	A9	B9	+12V
IOCHRDY	A10	B10	NC
AEN	A11	B11	SMEMW
A19	A12	B12	SMEMR
A18	A13	B13	IOW
A17	A14	B14	IOR
A16	A15	B15	NC
A15	A16	B16	NC
A14	A17	B17	NC
A13	A18	B18	NC
A12	A19	B19	Pull-Up
A11	A20	B20	NC
A10	A21	B21	IRQ7
A9	A22	B22	IRQ6
A8	A23	B23	IRQ5
A7	A24	B24	IRQ4
A6	A25	B25	IRQ3
A5	A26	B26	NC
A4	A27	B27	Pull-Down
A3	A28	B28	Pull-Up
A2	A29	B29	VDD50
A1	A30	B30	NC
A0	A31	B31	GND
GND	A32	B32	GND

GND	D1	C1	GND
NC	D2	C2	SBHE
NC	D3	C3	A23
IRQ10	D4	C4	A22
IRQ11	D5	C5	A21
IRQ12	D6	C6	A20
IRQ15	D7	C7	A19
IRQ14	D8	C8	A18
NC	D9	C9	A17
NC	D10	C10	MEMR
NC	D11	C11	MEMW
NC	D12	C12	D8
NC	D13	C13	D9
NC	D14	C14	D10
NC	D15	C15	D11
NC	D16	C16	D12
VDD50	D17	C17	D13
Pull-Up	D18	C18	D14
GND	D19	C19	D15
GND	D20	C20	NC

Pull-Up :Pull-up 10K resistor at +5V

Pull-Down :Pull-down 10K resistor at GND

2.16. RESET (JP11)

Pin-Outs Table:

1	nMR
2	GND

JP11 :Cosed JP11 reset the system

2.17. LED' S (D2、 D3、 D8、 D9)

The led designed to show the CPU status and power status.

D2 : CPU LED

D3 : CPU LED

D8 : VDD50 LED

D9 : VDD33 LED

2.18. AUDIO (J1、J2、J3)

A AC' 97 audio CODEC is used to support the audio features of the SBC-9315. Audio inputs and output supported by the CS4202 are stereo line out and line in ,and it supported a mono microphone input.

J1 : line out

J2 : mic

J3 : line in

2.19. PWM (JP7)

Pin-Outs Table:

1	GND
2	PWMOUT

2.20. Ethernet Port (RJ45)

The EP9315 has a Ethernet MAC,the MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported.Features include:

- Supports 1/10/100 Mbps transfer rates for home /small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

The EP9315 Ethernet LAN controller incorporates all the logic needed to interface directly to any MII compatible Ethernet PHY chip. A low-power Micrel KS8721 chip is used to implement the Ethernet PHY function and an integrated RJ-45 connector with built-in 10/100 transformer and LED indicators completes the Ethernet sub-system.

2.21. Real-Time Clock

The SBC-9315 has an option for a real-time clock (RTC). This option (PCF8563) is a CMOS real-time clock/calendar optimized for low power consumption This module contains the 3.0 V lithium battery, 32.768 kHz crystal, and a RTC chip . It is low back-up current; typical 0.25 mA at VDD = 3.0 V and Tamb = 25 °C

2.22. Watchdog Timer

The SBC-9315 implements a watchdog timer (WDT) unit. The WDT can be used to prevent a system “hanging” due to a software failure. The WDT causes a full system reset when the WDT times out, allowing a guaranteed

recovery time from a software error. To prevent a WDT timeout, the application must periodically “feed” the WDT by writing a specific value to a specific memory location.

The WDT Control register must be initialized with the timeout period desired. This may be as short as 1.6 seconds. After the WDT has been enabled, the WDT counter starts counting. The application software can reset this counter at any time by “Feeding the WDT”.If the WDT counter reaches the timeout period, then a full system reset occurs.

2.23. CPLD (CN15)

Use it to program CPLD IC.

Pin-Outs Table:

TCK	1	2	GND
TDO	3	4	VDD33
TMS	5	6	NC
NC	7	8	NC
TDI	9	10	GND

Revision History

Version	Modifications
Rev 1.0	Initial version
Rev 2.0	
Rev 3.0	Update all